IN THE SPECIFICATION:

Please replace the title of the invention with the following amended title:

METHOD AND APPARATUS FOR HANDLING INTERRUPTS USING A SET OF INTERRUPT SERVERS ASSOCIATED WITH PRESENTATION CONTROLLERS

Please replace the abstract of the invention with the following amended abstract:

A method, apparatus, and computer instructions for managing interrupts using a set of presentation controllers. ~~Each interrupt presentation controller contains a set of interrupt management areas (one for each processor associated with the interrupt presentation controller – the combination of interrupt management area and processor is known as an "interrupt server").~~ A first interrupt server is identified in the set of interrupt servers to handle the interrupt in response to receiving an interrupt signal. The set of interrupt servers constituting a server pool are linked in a circular list using a set of identifiers ~~found in the interrupt management area of the interrupt servers within the set of presentation controllers~~. The message representing the interrupt is sent to a second interrupt server, such as in a second presentation controller in the set of presentation controllers based on an identifier identifying the second interrupt server in the set of interrupt servers, if the first interrupt server is unable to handle the interrupt. The identifier is found within the first interrupt controller. The interrupt is passed to different interrupt servers potentially associated with different presentation controllers within the circular list ~~until one of the interrupt servers is able to process the interrupt or until all servers in the list have passed the interrupt message – at which time the interrupt message is rejected back to the interrupt source controller for later representation~~.

Please replace the third full paragraph on page 5-6 of the application, with the following:

Shortcomings in these types of interrupt subsystems involve the use of a central collection of logic that stores the identification of processors selected for handling interrupts. The problem with this type of interrupt subsystem is that the central collection of logic has to increase in size and complexity as the total number of processors that are supported grows. As a result, the central collection of logic becomes large and expensive having to be sized for the maximum number of processors that the system can support, even though most systems are not that large.

Further, this central collection of logic also becomes a single point of failure for the entire interrupt subsystem. As a result, duplication or redundancy is required to guard against such failures.

Please replace the second full paragraph on page 9 of the application, with the following:

In these examples, interrupt source controllers **104**, **106**, and **108** are connected to interconnect fabric **102**. These components receive interrupt signals from components, such as adapters **110**, **112**, and **114**. These components generate interrupt messages or interrupt signals through wires that connect the components to interrupt source controllers **104**, **106**, and **108**. Of course, other types of devices or components other than adapters also may be connected to these controllers to generate interrupt signals.

Please replace the first full paragraph on page 11 of the application, with the following:

The present invention uses the interrupt subsystem architecture in data processing [[sub]]system **100** in **Figure 1** to more efficiently assign interrupts to different processors with respect to prior art systems. When interrupt signals are received from a component, such as adapter **110**, by an interrupt source controller, such as interrupt source controller **104**, the interrupt is received over a line, which is associated with a particular interrupt server number.

Please replace the first full paragraph on page 14 of the application, with the following:

Interrupt presentation controller **204** contains the interrupt management area for an interrupt server – represented is the subset of this area relevant to this invention, including interrupt source number **228**, priority **230**, (collectively known as the XIRR as described above) and link register **232**; similarly, interrupt presentation controller **206** includes interrupt source number **234**, priority **236**, and link register **238**; interrupt presentation controller **208** includes interrupt source number **240**, priority **242**, and link register **244**; and interrupt presentation controller **210** contains interrupt source number **246**, priority **248**, and link register **2[[50]]49**.

Please replace the second full paragraph on page 16-17 of the application, with the following:

In these examples, interrupt signals are sent to interrupt source controller **202** through signal lines **250** and **252**. The interrupt generated on signal line **252** results in an interrupt message being sent to the interrupt management area in interrupt presentation controller **204**. The interrupt message is sent to this interrupt presentation controller because the interrupt server number points to this particular interrupt server. The address in link register **232** points back to the interrupt management area in interrupt presentation controller **204**. In this illustrative example, only the interrupt server associated with interrupt presentation controller **204** is present in this particular circular list. The interrupt signal generated on signal line **250** results in an interrupt message being sent to the interrupt management area of interrupt presentation controller **206**. In this example, three interrupt servers located in three interrupt presentation controllers are in the circular list. These interrupt presentation controllers are interrupt presentation controllers **206**, **208**, and **210**. In this example, link register **238** in interrupt presentation controller **206** points to interrupt presentation controller **210**. Link register **2[[50]]49** in interrupt presentation controller **210** points to interrupt presentation controller **208**. In turn, link register **244** in interrupt presentation controller **208** points back to interrupt presentation controller **206** to form the circular list or loop according to a preferred embodiment of the present invention.

Please replace the third full paragraph on page 21-22 of the application, with the following:

Next, an interrupt message is sent to an interrupt server in an interrupt presentation controller identified within the interrupt server number (step **304**). Thereafter, a determination is made as to whether the interrupt message has been accepted (step **306**). If the interrupt message is not accepted, the process waits for a period of time (step **308**) then proceeds to represent the interrupt at a later time by looping back to step **302**. This process is known as "interrupt rejection and representation" and is implemented using other mechanisms such as those in United States Patent No. 5,701,495 or United States Patent No. 6,430,643, which are incorporated here and by reference. Returning again to the determination made in step **306**, if the interrupt message is accepted, the process ends.